Development of Domain Wall Type Spin Memristor toward Analogue Neuromorphic Computing

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Recent evolution of Artificial Intelligence (AI) is bringing drastic changes to society and industry. On the other hand, the rapid increase of its energy burden has become an urgent issue. From this viewpoint, an analogue neuromorphic computing have attracted much attention due to its extremely low-power and high-performance neural-network (NN) computing ability [1]. Memristors play key roles for realizing neuromorphic devices. It can store a synaptic weight of NN as an analog resistance state. For example, large-scale parallel multiply-accumulate (MAC) operation can be executed by applying an electric current flow to a memristor array. Memories-based spiking neural network devices have also been studied to accelerate the computational processing power with keeping power consumption. Phase change memory (PCM) and Resistive-RAM (ReRAM) are well-known elements in this field. A magnetic domain wall (DW) type memristor (spin-memristor) is another promising candidate for artificial synapses because of its typical conductance change behavior, non-volatility, high speed and high endurance operations. Numerical simulations show potential advantages of the spin-memristor [2]. However, an element-level development has not been well established. The elements have been well studied for a high-speed domain wall (DW) type MRAM, but not so much for memristors. In this presentation, we introduce our recent efforts to develop the spin-memristor for the neuromorphic application. The concept of the spin-memristor was verified by preparing a DW type magnetic tunneling junction (MTJ). Three-terminal top-pinned type MTJs were fabricated on a Si substrate. The stacking layer was Si wafer /buffer /DW layer /CoFeB Free layer /tunnel barrier /CoFeB Reference layer /synthetic antiferromagnetic (SAF) pinned layer. A pulse generator and a source measure unit are used for driving the DW and for measuring the resistance of MTJs. A linear and symmetric conductance response (Fig. 1), which was desirable for the artificial synapse, was experimentally demonstrated in the element level as expected [3]. A good NN computation adaptability was confirmed using a numerical simulation with its simplified element model. In addition, we also developed a 3-terminal element having SAF-type magnetic fixed layer at the one side of DW layer (Fig. 2), and successfully controlled the element initialization process just by applying an external magnetic field [4]. Since this structure allows us to initialize multiple elements by a simple procedure, it becomes helpful to realize an array level system and a mass-production in the future. The prototype element suggested a low power operation potential which may be at least comparable to other memristive elements such as PCM and ReRAM.

References
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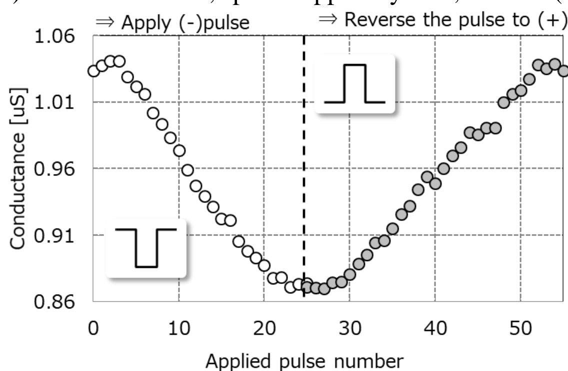

Fig.1 Symmetric conductance response as a function of driving current pulse

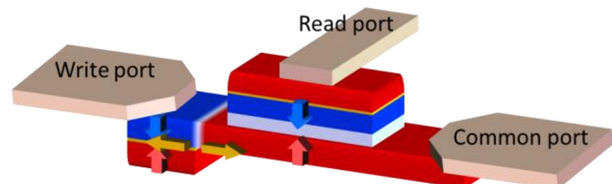

Fig.2 Schematic illustration of the element with SAF-type magnetic fixed layer